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1 Computing the minimum DNF representation of boolean functions defined by intervals

Baruch Schieber, Daniel Geist, Ayal Zaks

August 2005 **Discrete Applied Mathematics**, Volume 149 Issue 1-3

Publisher: Elsevier Science Publishers B. V.

Additional Information: full citation, abstract, references, index terms

For any two n-bit numbers $a \leq b$ define the Boolean function $f[a,b] : \{0, 1\}^n \rightarrow \{0, 1\}$ to be the function for which $f[a,b]\ (x) = 1$ if and only if x is the binary representation of a number in the interval $[a, b]$. We consider the disjunctive normal form representation of such functions, and show how to compute such a representation with a minimum number of disjuncts in linear time. We also show how ...

Keywords: DNF, automatic test generation, boolean function, constraint satisfaction, disjunctive normal form

2 Semantic control in continuous systems: applications to aerospace problems

Daniel Geist, E. Y. Rodin

January 1990 Doctoral Thesis

Additional Information: full citation

3 Semi-Formal Test Generation for a Block of Industrial DSP

Julia Dushina, Mike Benjamin, Daniel Geist

March 2001 **Proceedings of the 19th IEEE VLSI Test Symposium**

Publisher: IEEE Computer Society

Full text available: Publisher Site Additional Information: full citation, abstract

This article describes an industrial application of the Genevieve test generation methodology. The Genevieve approach [1] uses formal techniques to generate test suites for specific design behaviour. The example, which is a part of the ST100 DSP, was chosen in order to highlight real life problems such as big data structures, complex control logic, and complex environments where it is difficult to determine how to drive the complete system to ensure a given behaviour in the unit under test.

4 RuleBase: Model Checking at IBM
Ilan Beer, Shoham Ben-David, Cindy Eisner, Daniel Geist, L. Gluhovsky, Tamir Heyman, Avner Landver, P. Paanah, Yoav Rodeh, G. Ronin, Yaron Wolfsthal
June 1997 **Proceedings of the 9th International Conference on Computer Aided Verification**
Publisher: Springer-Verlag
Additional Information: full citation, citings

5 Methodology and System for Practical Formal Verification of Reactive Hardware
Ilan Beer, Shoham Ben-David, Daniel Geist, Raanan Gewirtzman, Michael Yoeli
June 1994 **Proceedings of the 6th International Conference on Computer Aided Verification**
Publisher: Springer-Verlag
Additional Information: full citation, citings

6 Efficient Model Checking by Automated Ordering of Transition Relation Partitions
Daniel Geist, Ilan Beer
June 1994 **Proceedings of the 6th International Conference on Computer Aided Verification**
Publisher: Springer-Verlag
Additional Information: full citation, citings

7 Symbolic Localization Reduction with Reconstruction Layering and Backtracking
Sharon Barner, Daniel Geist, Anna Gringauze
July 2002 **Proceedings of the 14th International Conference on Computer Aided Verification**
Publisher: Springer-Verlag
Additional Information: full citation, citings

8 Achieving Scalability in Parallel Reachability Analysis of Very Large Circuits
Tamir Heyman, Daniel Geist, Orna Grumberg, Assaf Schuster
July 2000 **Proceedings of the 12th International Conference on Computer Aided Verification**
Publisher: Springer-Verlag
Additional Information: full citation, citings

9 "Have I written enough Properties?" - A Method of Comparison between Specification and Implementation
Sagi Katz, Orna Grumberg, Daniel Geist
September 1999 **Proceedings of the 10th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods**
Publisher: Springer-Verlag
Additional Information: full citation, citings

10 Coverage-Directed Test Generation Using Symbolic Techniques

Daniel Geist, Monica Farkas, Avner Landver, Yossi Lichtenstein, Shmuel Ur, Yaron Wolfsthal
November 1996 **Proceedings of the First International Conference on Formal Methods in Computer-Aided Design**
Publisher: Springer-Verlag
Additional Information: full citation, citings

11 Model Checking at IBM
Shoham Ben-David, Cindy Eisner, Daniel Geist, Yaron Wolfsthal
March 2003 **Formal Methods in System Design**, Volume 22 Issue 2
Publisher: Kluwer Academic Publishers
Full text available: Publisher Site Additional Information: full citation, abstract, references, index terms, review

Over the past nine years, the Formal Methods Group at the IBM Haifa Research Laboratory has made steady progress in developing tools and techniques that make the power of model checking accessible to the community of hardware designers and verification engineers, to the point where it has become an integral part of the design cycle of many teams. We discuss our approach to the problem of integrating formal methods into an industrial design cycle, and point out those techniques which we have f ...

Keywords: formal methods, formal verification, model checking

12 On the Effective Deployment of Functional Formal Verification
Yael Abarbanel-Vinov, Neta Aizenbud-Reshef, Ilan Beer, Cindy Eisner, Daniel Geist, Tamir Heyman, Iris Reuveni, Eran Rippel, Irit Shitsevalov, Yaron Wolfsthal, Tali Yatzkar-Haham
July 2001 **Formal Methods in System Design**, Volume 19 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We examine IBM's exploitation of formal verification using RuleBase—a formal verification tool developed by the IBM Haifa Research Laboratory. The goal of the paper is methodological. We identify an integrated methodology for the deployment of formal verification which involves three complementary modes: architectural verification, block-level verification, and design exploration.

Keywords: formal verification, hardware verification, model checking

13 Semi-formal test generation with genevieve
Julia Dushina, Mike Benjamin, Daniel Geist
June 2001 **Proceedings of the 38th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(146.93 KB) Additional Information: full citation, abstract, references, index terms

This paper describes the first application of the Genevieve test generation methodology. The Genevieve approach uses semi-for-mal techniques derived from "model-checking" to generate test suites for specific behaviours of the design under test. An "interest-ing" behaviour is claimed to be unreachable. If a path from an ini-tial state to the state of interest does exist, a counter-example is generated. The sequence of states specifies a test for the desired behaviour. ...

14 A study in coverage-driven test generation
Mike Benjamin, Daniel Geist, Alan Hartman, Gerard Mas, Ralph Smeets, Yaron Wolfsthal
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(67.02 KB) Additional Information: full citation, references, citings, index terms

Keywords: formal models, functional verification, test generation, transition coverage

15 A methodology for the verification of a "system on chip"
Daniel Geist, Giora Biran, Tamara Arons, Michael Slavkin, Yvgeny Nustov, Monica Farkas, Karen Holtz, Andy Long, Dave King, Steve Barret
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(63.75 KB) Additional Information: full citation, references, citings, index terms

Keywords: systems on chip, test and debugging, verification

16 Adjacency of the 0–1 knapsack problem
Daniel Geist, Ervin Y. Rodin
November 1992 **Computers and Operations Research**, Volume 19 Issue 9
Publisher: Elsevier Science Ltd.
Additional Information: full citation, index terms

17 Combining System Level Modeling with Assertion Based Verification
Anat Dahan, Daniel Geist, Leonid Gluhovsky, Dmitry Pidan, Gil Shapir, Yaron Wolfsthal, Lyes Benalycherif, Romain Kamdem, Younes Lahbib
March 2005 **Proceedings of the Sixth International Symposium on Quality of Electronic Design (ISQED'05) - Volume 00**
Publisher: IEEE Computer Society
Full text available: Publisher Site Additional Information: full citation, abstract

Assertion-Based Verification (ABV) using the PSL language is currently gaining acceptance as an essential method for functional verification of hardware. A basic technique to implement ABV is to embed temporal assertions in RTL code. This paper describes the use of a PSL-based ABV methodology in a C++-based system level modeling and simulation environment. We describe the considerations of porting a tool which translates PSL to VHDL/Verilog, to support C++, a language which was designed for soft ...

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D Geist, M Farkas, A Landver, Y Lichtenstein, S Ur ... - Proc. of the International Conference in Formal Methods in ..., 1996 - portal.acm.org
... Pages: 143 - 158. Year of Publication: 1996. ISBN:3-540-61937-2. Authors, **Daniel Geist**, Monica Farkas, Avner Landver, Yossi Lichtenstein, Shmuel Ur, Yaron Wolfsthal ...
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[BOOK] Methodology and System for Practical Formal Verification of Reactive Hardware
I Beer, S Ben-David, D Geist, R Gewirtzman, M ... - Proceedings of the 6th International Conference on Computer ..., 1994 - Springer-Verlag London, UK
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M Benjamin, D Geist, A Hartman, Y Wolfsthal, G Mas ... - PROC DES AUTOM CONF. pp. 970-975. 1999, 1999 - doi.ieeecomputersociety.org
2. INTRODUCTION There is now widespread acceptance in the EDA community that the resources devoted to functional verification are increasing ...
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D Geist, G Biran, T Arons, M Slavkin, Y Nustov, M ... - PROC DES AUTOM CONF. pp. 574-579. 1999, 1999 - doi.ieeecomputersociety.org
Daniel Geist, Giora Biran, Tamara Arons, Michael Slavkin, Yvgeny Nustov, Monica Farkas, Karen Holtz IBM Haifa Research Lab MATAM Advanced Technology Center ...
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"Have I written enough Properties?" - A Method of Comparison between Specification and ... - group of 7 »
S Katz, O Grumberg, D Geist - LECTURE NOTES IN COMPUTER SCIENCE, 1999 - Springer
Abstract. This work presents a novel approach for evaluatingthe qual- ity of the model checkingprocess. Given a model of a design (or imple- mentation) and ...

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Symbolic Localization Reduction with Reconstruction Layering and Backtracking - group of 7 »
S Barner, D Geist, A Gringauze - CAV, 2002 - Springer
Abstract. Localization reduction is an abstraction-refinement scheme for model checking which was introduced by Kurshan [12] as a means for tackling state ...
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